



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,391	08/06/2003	Vladimir Rodov	ESD1.PAU.01	1187
7590	09/29/2004		EXAMINER	
David L. Henty Myers Dawes Andras & Sherman, LLP Suite 1150 19900 MacArthur Blvd. Irvine, CA 92612			WARREN, MATTHEW E	
			ART UNIT	PAPER NUMBER
			2815	
			DATE MAILED: 09/29/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/635,391	RODOV ET AL.
	Examiner	Art Unit
	Matthew E Warren	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 06 August 2003.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-39 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 12-21 is/are allowed.  
 6) Claim(s) 1-11 and 22-39 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date 6/17/04.
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Objections***

Claim 35 is objected to because of the following informalities: the claim contains the limitation of "the switch structure." There is insufficient antecedent basis for the limitation in the claim. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6-9, 30, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Pan (US 6,259,139 B1).

In re claim 1, 30, and 35, Pan shows (fig. 3A) an integrated circuit incorporating an Electrostatic Discharge (ESD) protection device comprising'; a semiconductor substrate (30); an electrical contact pad (32); an ESD switch coupled to the pad and having an active device region (36) formed in the semiconductor substrate; and a thermal energy absorbing region (30) (col. 4, lines 29-44) formed in the semiconductor substrate in thermal contact with said active device region made from a material substantially more resistant to thermo-mechanical expansion than said active device region. A core circuit (13 in fig. 1) comprising a plurality of devices having electrical

connectors and active device regions is formed in the semiconductor substrate with electrical insulators. The ESD circuit further comprises electrical connectors (396), insulator regions (385), passive components, wherein the substrate material (30) is composed of a material more resistant to thermo-mechanical damage than the corresponding structure in the core circuit. The substrate material is more resistant to thermo-mechanical damage heat is absorbed by the substrate, thus protecting the ESD circuit from heat (col. 4, lines 38-40).

In re claims 6-9, Pan discloses (col. 4, lines 29-44) that the ESD switch is a transistor, that the transistor is a MOSFET having a source, drain, and channel, and that ESD switch has diodes. In figure 3A, the thermo-mechanical absorbing region (30) is in direct contact with the active device region (36).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-5, 10, and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (US 6,259,139 B1) as applied to claim 1 above, and further in view of Yatsuo et al. (US 6,353,236 B1).

In re claims 2-5, 10, and 32-34 Pan does not show the specific properties of the material more resistant to thermo-mechanical expansion, however, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to use a known material having the desired properties, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Yatsuo discloses (col. 5, lines 53-65) an ESD protection device/absorber using SiC as described in claim 10 to provide protection from a power surge and while providing thermal resistance. The SiC layer has a melting temperature higher than 2000 degrees K as stated in claim 3 and inherently has the same properties as stated in claims 2, 4, and 5 since the material is the same as the instant invention. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor thermal energy absorbing layer of Pan by using SiC as taught by Yatsuo to provide ESD protection and resistance to thermal-mechanical breakdown, ultimately increasing the endurance of the protections circuit.

Claims 11 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (US 6,259,139 B1) as applied to claim 1 above, and further in view of Uenishi (US 2002/0070424 A1).

In re claims 11 and 31, Pan shows all of the elements of the claims except the ESD switch including a resistor or capacitor as the passive component. Uenishi shows. (fig. 1) a resistor (3) to provide ESD protection coupled with a thermal energy absorbing region (6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ESD switch of Pan by adding a resistor to

the thermal energy absorbing region as taught by Yatsuo to provide adequate heat and electrostatic transfer during an ESD event.

Claims 22-29 and 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (US 6,259,139 B1 in view of Yatsuo et al. (US 6,353,236 B1).

In re claims 22 and 36, Pan shows (fig. 3A) and discloses (col. 3, line 30 – col. 4, line 28) a method of fabricating an ESD devices comprising a semiconductor substrate (30); an electrical contact pad (32); an ESD switch coupled to the pad and having an active device region (36) formed in the semiconductor substrate; and a thermal energy absorbing region (30) (col. 4, lines 29-44) formed in the semiconductor substrate in thermal contact with said active device region made from a material substantially more resistant to thermo-mechanical expansion than said active device region. A core circuit (13 in fig. 1) comprising a plurality of devices having electrical connectors and active device regions is formed in the semiconductor substrate with electrical insulators. The ESD circuit further comprises electrical connectors (396), insulator regions (385), passive components, wherein the substrate material (30) is composed of a material more resistant to thermo-mechanical damage than the corresponding structure in the core circuit. The substrate material is more resistant to thermo-mechanical damage heat is absorbed by the substrate, thus protecting the ESD circuit from heat (col. 4, lines 38-40). Pan does not show the specific properties of the material more resistant to thermo-mechanical expansion, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a known material having the desired

properties, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Yatsuo discloses (col. 5, lines 53-65) an ESD protection device/absorber using SiC as to provide protection from a power surge and while providing thermal resistance. The SiC layer has a melting temperature higher than 2000 degrees K as stated and inherently has the same properties as stated in claims 2, 4, and 5 since the material is the same as the instant invention. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor thermal energy absorbing layer of Pan by using SiC as taught by Yatsuo to provide ESD protection and resistance to thermal-mechanical breakdown, ultimately increasing the endurance of the protections circuit.

In re claims 23-25 and 37-39 ,Yatsuo discloses (col. 5, lines 53-65) that an ESD protection device/absorber using SiC to provide protection from a power surge while providing thermal resistance. The SiC layer has a melting temperature higher than 2000 degrees K as stated and inherently has the same properties as stated in claims 24, 25, and 37-39 since the material is the same as the instant invention.

In re claims 26-29, Yatsuo shows (fig. 1) that a grounded back contact (4) is electrically coupled to the substrate (2) and that the active device comprises a thermo-mechanical energy sink (1) of silicon carbide (hard carbon).

***Allowable Subject Matter***

Claims 12-21 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art references, alone or in combination, do not an integrated circuit incorporating an Electrostatic Discharge (ESD) protection device comprising a first connector formed of a first electrically conductive material connecting a plurality of active devices; an ESD switch coupled to a pad, at least in part via a second connector, said second connector electrically connected to the ESD switch comprising material more resistant to thermo-mechanical expansion than said first connector formed of said first electrical conductive material wherein the second connector extends away from the substrate a distance at least equal to one-half of the length of the active device region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bryant et al. (US 6,436,744 B1) and Sabin et al. (US 6,734,093 B1) also disclose ESD protection devices having thermal energy absorbing materials.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571)

Art Unit: 2815

272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

*meaw*

September 27, 2004